REMARKS

In the Office Action mailed November 22, 2005, claims 1-17 and 21-27 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 1-4, 6-27 are rejected under 35 USC §102(e) as being anticipated by Nadeau-Dostie et al., US Patent 6,829,730, (hereinafter "Nadeau-Dostie"). Claim 5 is rejected under 35 USC §103(a) as being obvious in view of Nadeau-Dostie.

Applicant gratefully acknowledges the telephone conference on February 15, 2006, and has amended the claims to overcome the rejections under 35 USC §112, second paragraph, and to put the claims in a condition for allowance, as discussed. In particular, Applicant has amended independent claims 1, 7, 11, 14 and 21 to more clearly indicate that the apparent length or size of the instruction register of the host JTAG TAP controller comprises a combination of the length or size of the instruction register of the host JTAG TAP controller and the length or size of an instruction register of an IP core JTAG TAP controller. Applicant respectfully submits that the claims as amended are no longer ambiguous and should be in allowable form.

Applicant also reiterates that the claims as drafted clearly distinguish over Nadeau-Dostie. Applicant points out that, in order to ensure that the length of each TAP group is as long as the master TAP (or host TAP) of Nadeau-Dostie, the master TAP has a fixed length that is selected based upon the length of the longest group of TAPS. That is, the number of bits of the instruction register of the master TAP is selected to be equal to the length of the instruction registers of the longest TAP group plus the number of bits necessary to select the TAP group. (Col. 7, lines 20-50). However, when a TAP group other than the master TAP is selected, elements of the instruction register of the master TAP may be used to "pad' the length of the instruction register of the TAP group in order to ensure that the length of the instruction register of the TAP group is as long as the instruction register of the master TAP. Applicant's claims clearly distinguish over Nadeau-Dostie, as will be described below with respect to each independent claim.

Independent Claim 1

Independent claim 1 is directed to a method for flexibly nesting JTAG TAP controllers for IP cores in a FPGA-based system-on-chip (SoC). In response to the rejection under 35 USC §112, second paragraph, Applicant has amended claim 1 to indicate that the apparent length of the instruction register of the host JTAG TAP controller comprises "a combination of the length of said instruction register of said host JTAG TAP controller and the length of an instruction register of said selected IP core JTAG TAP controller." Applicant respectfully submits that independent claim 1 is now in allowable form.

Applicant further submits that Nadeau-Dostie fails to disclose or suggest extending the apparent length of the instruction register as claimed. That is, Nadeau-Dostie teaches using a fixed length instruction register for a master TAP, and modifying a core TAP to ensure that the instruction register of the core TAP is the same length as the instruction register of the master TAP. Accordingly, Nadeau-Dostie fails to disclose or suggest extending the apparent length of the instruction register of the host JTAG TAP, as claimed in independent claim 1. Applicant submits that claim 1, and dependent claims 2-6, clearly distinguish over Nadeau-Dostie, and respectfully request reconsideration of the claims.

Independent Claim 7

Independent claim 7 is directed to a method for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. Applicant has also amended claim 7 to overcome the rejection under 35 USC §112, second paragraph, by indicating that the apparent register size of an instruction register of the host JTAG TAP controller comprises "the combined size of an instruction register for said at least one IP core JTAG TAP controller and the size of said instruction register of said host JTAG TAP controller." Applicant respectfully submits that independent claim 7 is now in allowable form.

Applicants also respectfully submit that claim 7 distinguishes over Nadeau-Dostie. In contrast to Applicant's claim 7, Nadeau-Dostie teaches using a fixed

register size of an instruction register based upon the largest register for any TAP or group of TAPS, but fails to disclose or suggest selecting an apparent size of an instruction register of a host JTAG tap controller, as described above. Accordingly, Applicant submits that claim 7 clearly distinguishes over Nadeau-Dostie, and that claim 7 and dependent claims 8-10 are allowable over Nadeau-Dostie.

Independent Claim 11

Claim 11 is directed to a system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. Applicant has amended claim 11 to overcome the rejection under 35 USC §112, second paragraph, by indicating that the apparent length of the instruction register of the host JTAG TAP controller comprises "a combination of a length of an instruction register of said IP core JTAG TAP controller and a length of said instruction register of said host JTAG TAP controller." Applicant respectfully submits that independent claim 11 is now in allowable form.

Applicants also respectfully submit that claim 11 distinguishes over Nadeau-Dostie. In contrast to Applicant's system of claim 11 having a selector for selecting at least one available bit to extend the apparent length of an instruction register of the host JTAG TAP controller, the master TAP disclosed in Nadeau-Dostie is fixed based upon the length of the longest TAP group. Nadeau-Dostie fails to disclose or suggest extending the apparent length of an instruction register of a host JTAG TAP controller. Accordingly, Applicant submits that claim 11 and dependent claims 12-13 clearly distinguishes over Nadeau-Dostie.

Independent Claim 14

Independent claim 14 is directed to a system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. Applicant has amended the claim to overcome the rejection under 35 USC §112, second paragraph, by indicating that the apparent register size of an instruction register of the host JTAG TAP controller comprises "a size of an instruction register of said at least one IP core JTAG TAP controller and a size of said instruction register of said host JTAG TAP

controller." Applicant respectfully submits that independent claim 14 is now in allowable form.

Applicant also respectfully submits that claim 14 distinguishes over Nadeau-Dostie. In contrast to Applicant's system of claim 14, the instruction register of the master TAP of Nadeau-Dostie does not disclose or suggest enabling the selection of an apparent register size of an instruction register of the host JTAG TAP controller, for the reasons set forth above. Accordingly, Applicant submits that claim 14 clearly distinguishes over Nadeau-Dostie, and that dependent claims 15-17 are allowable over Nadeau-Dostie for the same reasons that claim 14 is believed allowable. Applicant respectfully requests reconsideration of the claims.

Independent Claim 18

Independent claim 18 is directed to a method for ensuring an information register length for nested JTAG TAP controllers for IP cores remains the same "before and after a configuration of an FPGA" in an FPGA-based system-on-chip (SoC). Applicant has amended claim 18 to correct a typographical error, and therefore obviating the rejection of claim 18. In particular, Applicant has amended claim 18 to indicate that the instruction registers for the IP cores are in series with the instruction register of the FPGA of the SoC. As set forth above, the instruction register of the master TAP of Nadeau-Dostie is not coupled in series with the instruction register of core JTAG TAPS. Rather, a predetermined number of elements of an instruction register of the master TAP are used as "padding registers" to ensure that the length of a selected core TAP or group of core TAPs is the same length as the fixed length master TAP.

Applicant further submits that Nadeau-Dostie fails to disclose or suggest (i) forming connections between FPGA JTAG logic and IP Core JTAG logic using a programmable interconnect, or (ii) emulating an instruction register of the IP core prior to configuration of the FPGA. There is no teaching or suggestion of programmable interconnects or the configuration of a programmable logic device, such as an FPGA, as claimed. Accordingly, Applicant respectfully submits that independent claim 18

and dependent claims 19-20 are allowable over Nadeau-Dostie, and respectfully requests reconsideration of the claims.

Independent Claim 21

Independent claim 21 is directed to a system for performing boundary scan functions on a plurality of IP cores. Applicant has amended the claim to overcome the rejection under 35 USC §112, second paragraph, by indicating that the apparent register size of the host JTAG TAP controller comprises "a combination of a size of an instruction register of the first JTAG TAP controller for each IP core of the plurality of IP cores and the size of the instruction register of the host JTAG TAP controller." Applicant submits that the claim as amended is in allowable form.

Applicant further submits that Nadeau-Dostie fails to disclose or suggest a host JTAG TAP controller comprising a selectable bit register enabling the selection of an apparent register size of an instruction register of the host JTAG TAP controller. Accordingly, Applicant respectfully submits that claim 21 and dependent claims 22-27 are allowable over Nadeau-Dostie, and respectfully requests reconsideration of the claims.

CONCLUSION

All claims are in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on February 27, 2006.

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